APPENDIX

Device Descriptions

Memory Devices

Several primary characteristics of memories serve to differentiate one type from another. Among those characteristics are the devices' functional sizes and method of storing information.

The device size refers to the number of functions, in this case bits of memory, resident on a chip. Early devices had 256 functions (binary digits, or bits) on a chip. The 1k (1 kilobit) device has 1024 (2^{10}) functions; the 4k, 4096 (2^{12}); the 16k, 16384 (2^{14}); and so on. The 1 megabit chip, the commercially available device with the greatest density, has 2^{20} functions per chip. It is important to note that the n^{th} generation can do anything the n^{th}-but-one can do, and more. Thus for a memory chip, "more is better." Further, the size designation captures a lot of information about the products. For instance, in general, a larger functional size implies a small line width (the distance between functions on a chip) and faster access times and lower operating temperatures, all desireable characteristics.

Random access memories (RAM) are broadly classified into the designations dynamic and static, the distinction being made based upon their operating characteristics, which in turn obtain because of their different methods of storing information.

Dynamic Random Access Memory

In greatly oversimplified terms, dynamic random access memory devices (DRAMs) store information in the form of capacitors. As voltage is passed across a capacitor's plates, it accumulates a charge. It loses that charge over time, and thus requires a pulse of energy every so often to "refresh" that charge and retain the information. We study here the evolution of DRAMs beginning with the 4k (four kilobit) device. Successive generations are the 16k, 64k, and 256k.

The aggregate demand for dynamic memory has been explosive, to say the least: it climbed from 1.6×10^7 bits in the first quarter of 1974 to 2.2×10^{13} in the fourth quarter of 1984.

Static Random Access Memory

Static random access memory devices (SRAMs) store information in transistors and, by virtue of their construction, do not require refreshing. The SRAM is more complicated, more difficult, and more expensive to manufacture than a DRAM of the same density. In effect, it moves some of the complexity from the circuit board onto the chip itself (the complexity that results from circuitry required to refresh the DRAM's memory.) Thus, the SRAM user can make a less complicated set of circuit boards, a simpler and cleaner product, internally.

The markets for SRAMs and DRAMs are not generally the same ones. SRAMs lag a generation or so behind in size. SRAMs are more useful in areas where speed is important but density of memory is not so critical. Thus large mainframe computers use

them in cache memory (the computer equivalent of short-term memory in humans.) Because they make other circuitry simpler, and thus improve field reliability, they are favored for many military applications. And, because they consume less power than DRAMs, they are useful in such products as portable or laptop computers. To date 4k, 16k, and 64k devices are in use.

At present there are 26 major competitors in the dynamic memory markets worldwide, including Japanese and European producers. IBM also produces memory, but is not included in the database, as that production is for internal consumption, and because the information is not publicly available. A number of Korean firms have also entered the market (although all have entered after the data period in this document.) There are 27 producers of SRAMs, at this writing.

Logic Devices

Microprocessors (MPUs) perform primary instructions and system control functions, but cannot operate with peripherals, external devices that make them effective. They are usually classified according to the bit length of the largest word they can address: four, eight, sixteen, or thirty-two.

A microcontroller (MCU) is a device which can operate in a standalone fashion. It usually has some sort of read-only memory with instructions on it, some general-purpose RAM read/write memory, and the microprocessor function. MCUs are classified similarly to MPUs, and four, eight, and sixteen-bit devices are in use.

There are other types of logic devices, but MPUs and MCUs, along with coprocessors, represent a large segment of the business of performing logical functions.

The competitive arena for logic devices is different in several important ways from that for memory devices. In the case of memory, more is virtually always preferred to less. In the case of logic devices, the notion of sufficiency obtains: If you are controlling a light switch, a 4-bit device is more than enough, and an eight-bit device is unnecessarily complex. Unlike DRAMs, each successive size generation of logic devices is not a perfect plug-in substitute for the ones before it, nor is it necessarily used in precisely the same way. It is a mistake to assume that an engineer who knows how to use an eight-bit microprocessor automatically knows how to use the sixteen-bit device. Furthermore, microprocessors do not stand alone, but require peripherals. The cost of modifying or rewriting software is such that the replacement of an earlier device with a later one is something a design engineer must carefully consider. For these reasons, the "generations" we consider are MPU and MCU, the MCU being the "mature" form of the device, within a given device size, in this case eight-bit devices.

Timing and Magnitude of Peak Shipments

Taking the time derivative of equation (14),

$$d/dt\ S_1(t) = d/dt[1-F(t-\tau_2]m_1F(t)+d/dtF(t)[1-F(t-\tau_2)]m_1, \quad (1A)$$

and, if a=q/p and b=p+q,

$$d/dt\ S1(t) = [\exp(bt)]^2 - 2\exp(bt) - a([\exp(b\tau 2)(a+1)]+1). \quad (2A)$$

Using the quadratic formula, and using t_2 and the estimates of p and q, we find t^* and $S_1(t^*)$. It is similarly possible albeit tedious to estimate the timing and magnitude of peak sales for each generation.